Concept and current status of data acquisition technique for GEM detector based SXR diagnostics

A. Wojenski, K. Pozniak, G. Kasprowicz, W. Zabolotny, A. Byszuk, P. Zienkiewicz, M. Chernyshova, T. Czarski
GEM detector principles

Measures:
• Photon energy
• Photon position

Construction:
• Different architectures (1D, 2D)

Requirements:
• High number of readout channels
• Narrow, fast analog pulses from stripes („event” resolution)
• High voltage power supply
• Gas supply
• Controlled environment

Image from: https://gdd.web.cern.ch/GDD/gemreadout.htm

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1st IAEA Technical Meeting FDPVA 2015, 1-3.06.2015, Nice, France
GEM detector principles

Structure of the T-GEM X-ray detector for JET plasma diagnostics
M. Chernyshova et al., Development of GEM gas detectors for X-ray crystal spectrometry, JINST, 2014

Assembled T-GEM detector with analog front end for JET plasma diagnostics

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GEM detector for JET plasma diagnostics

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Output from the system
Tungsten spectrum and time evolution of the plasma discharge

K. T. Pozniak, FPGA based charge fast histogramming for GEM detector, SPIE, 2013
M. Chernyshova et al., Development of GEM gas detectors for X-ray crystal spectrometry, JINST, 2014
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GEM detector
Multiple channels

PCI-Express Switch 8-to-1

USB configuration link
PCI-Express interface

PC unit

Control software
Processing and acquisition software

Signal acquisition section (64 channels)
Backplane board

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Signals from GEM detector (up to 16)

Analog Front End Radiation Hard board

Configuration Links (LVDS)

Analog-Digital Front End board

Configuration links

Analog-Digital Front End board

Signals from GEM detector (up to 16)

Analog-Front End Radiation Hard board

Signals from GEM detector (up to 16)

Analog-Front End Radiation Hard board

Signals from GEM detector (up to 16)

Analog-Front End Radiation Hard board

Configuration link

Analog signal (after preprocessing)

Fast serial interface (SERDES)

Readout section

PCI-Express interface

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System overview (prototype)
System overview (prototype)

GEM detector

High voltage power supply
System overview (prototype)

AFE boards
System overview (prototype)

Backplane board
System overview (prototype)
System architecture

Key parameters AFE-RH board

- Configurable analog path (e.g. direct readout, pulse counting)
- Board test and calibration pulse circuit
- Offset calibration
- Designed to be radiation hard
- Fast, LVDS serializers for data transmission between AFE-RH and ADFE

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System architecture
Key parameters ADFE board

- 16 analog input channels with 125 MHz sampling speed (8 ns resolution)
- Offset calibration for each channel
- Analog path configuration (e.g. gain)
- Board protection circuit
- Fast, LVDS serializers for data transmission between AFE-RH and ADFE
System architecture - Backplane

- Up to 4 ADFE slots
- Artix7 FPGA
- SDRAM DDR3
- 4 High-speed Gigabit Serial Links (GTP) – connections between boards
- 1 High-speed Serial Interface for System Controller (e.g. PCIe, Ethernet)
System architecture – Protection board

- Independent board
- Operated by separate FPGA
- Continuous monitoring of:
  - Gas
  - Cooling (liquid)
  - Temperature
  - Over-current
  - High voltage
  - Pressure
  - Magnetic field
  - Humidity

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Firmware

- Configuration and management based on Wishbone standard
- Two versions implemented:
  - 64 channels independent signal recorders (1024 samples per channel) with global trigger (v1)
  - 64 channel fast integration algorithm with DDR3 memory storage (v2) – to be tested in next few days
- Data download through PCI-Express link

**Fast data acquisition algorithms**

- Comparator
- Raw signal from ADC channel
- Threshold value for the channel
- Fast signal recorder
- Data acquisition control block
- Fast digital charge integrator
- Multiplexer
- DDR3 memory
- Readout by PC
- PCI-Express interface

**Event Rates**
- 450kHz event rate from 16 channels (around 112.5 kHz from all 64 channels)
- 4.5 MHz event rate from 16 channels (around 1.125 MHz from all 64 channels)

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Data throughput requirements

- Each backplane board supports up to 64 measurement channels.
- Data transfer in FW v2: \(128\text{ bits} @ 1 \text{ MHz} \approx 1.20 \text{ Gbps}\)
- Expected data bursts (per 64 channels):
  - Normal mode (8 channel cluster):
    \(256 \text{ bits} @ 1\text{MHz} \approx 0.24 \text{ Gbps}\)
  - Peak value (all channels activated):
    \(2048 \text{ bits} @ 1\text{MHz} \approx 2 \text{ Gbps}\)

Data bandwidth

- PCI-Express Gen2: 64Gbps \((\approx 8 \text{ GB/s})\)
  Several PCI-E links used – shared bandwidth
- DDR3 memory: 24 Gbps \((\approx 3 \text{ GB/s})\)
  real: 21.6 Gbps \((\approx 2.7 \text{ GB/s})\)
- Optimization of data acquisition path and algorithms is most important in term of maximum event rate processing
- Special thanks to D. Mazon and CEA-Cadarache team for providing technical data about WEST tokamak

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High photon rates
Laser experiment at CELIA-Bordeaux

Special thanks to D. Batani, K. Jakubowska and rest of CELIA-Bordeaux team

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High event rates - multievents

- Occurs with very high event rate – e.g. plasma generated by laser (CELIA experiment)
- Overlapping of two signals – currently rejected by algorithm
- Modification of algorithm and/or analog front-end data path
- Can’t use constant time window – significant improvement in data rate handling

T. Czarski, K. Malinowski, A. Wojenski, “The test of GEM detector for laser-plasmas diagnostics in the CELIA laboratory with the ECLIPSE laser”, Scientific Report
Multievent algorithm

Registered signal with several events overlapping


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Multievent algorithm

Original pulses used to create superposition


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Multievent algorithm

Signals after reconstruction algorithm

Multievent algorithm

Reconstructed signals over original pulses

Very low error rate


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Software

- Modular framework – flexible implementation
- Easy interfacing with external components like GUI or software wrappers
- Used for:
  - Startup configuration of the system
  - System self-check
  - User-setup of the running system
  - Further online system management and diagnostics
  - Fast data download and parsing (mostly to easily diagnose the system)

Control unit alternatives

- Zynq SoC containing FPGA and Cortex-A9 core
- Linux operating system
- Small, portable
- Gigabit links
- Possible to provide fast data transmission using gigabit transceivers
- Fiber transmission over long distances
- Diagnostics and setup of the system
- Fast data analysis (technical)

Images from: http://zedboard.org/product/picozed
http://www.sfpopticaltransceiver.com

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Applications

KX1 spectrometry measurement system installed at JET

In collaboration with IPPLM, UW and JET (A. Shumack)

Tomography measurement system Currently under development

In collaboration with CEA Cadarache (D. Mazon and A. Jardin), IPPLM, WUT and NCU

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- K. T. Pozniak, et al., FPGA based charge fast histogramming for GEM detector, SPIE vol. 8903, 2013
- A. Wojęński, et al., GEM-2D detector based reconfigurable measurement system for hot plasma diagnostics, Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms, special issue – under review

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Thank you for attention

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